Calibration of the reference CTRIs in CCR and HCA442 for CNGS time transfer

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Abstract

This document explains the calibrations made at CERN between the reference CTRIs in CCR and HCA442 used for the CNGS beam time-stamp.

1 Introduction

The PPS output from the PolarRX is tagged by a CTRI installed in cfc-ccr-ctpps and driven by the SPS timing. This time-stamp is used as reference to translate from the SPS time to the PolarRX time. The proton spill acquisitions are time stamped with a different CTRI installed in HCA442 and also connected to the the SPS timing. As the cabling to both CTRIs remains stable the time offsets between both modules remains stable as well.

This delay has been calibrated in 2009, 2010 and 2011 with the following results:

$$-- > \text{CTRI VHDL Apr/2008}$$

$$\delta(2009)_3 = 10084.3ns \pm 2ns \quad (1)$$

$$\delta(2010)_3 = 10084.3ns \pm 2ns \quad (2)$$

$$-- > \text{CTRI VHDL Dec/2010 version change}$$

$$\delta(01/01/2011 - 19/04/2011)_3 = 10081ns \pm 2ns \quad (3)$$

$$-- > \text{Second CTRI connected to SPS timing}$$

$$\delta(19/04/2011)_3 = 10077ns \pm 2ns \quad (4)$$

2 Procedures

The timing link between the CCR and HCA442 has been calibrated using two methods, first a traveling cesium clock (CS4000) between 2008-2011 and since July 2011 with a calibration fiber. The traveling clock method is simple and direct. The accuracy is dictated by the stability of the traveling clock and the GPS reciver driving the timing system. The fiber calibration, as explained in Section 10 relies on the creation of a fully symmetric path between the points under calibration. The advantage of this method is that it allows a permanent monitoring of the transmission delay.

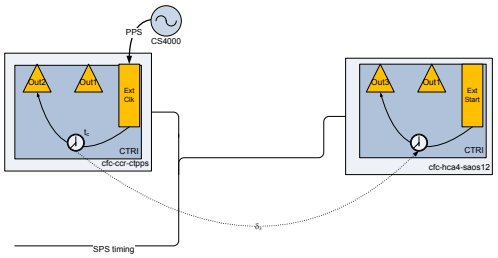

Figure 1: CS4000 PPS tagged at the CCR.

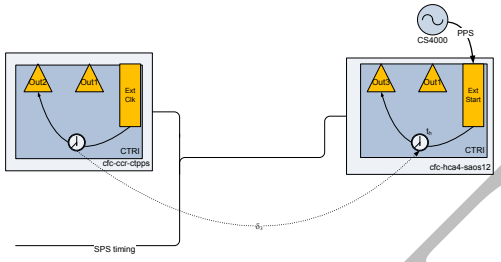

Figure 2: CS4000 PPS tagged at HCA442.

3 Traveling clock method

The reference CTRIs in HCA442 and CCR are frequency locked to the same UTC time base. There is an offset due to transmission delays between both time-bases that remains unknown if left uncalibrated of the order of the $10\mu s$. In the travelling clock callibration a PPS generated by the CS4000 is tagged by the CTRI in cfc-ccr-ctpps. The CS4000 is taken battery powered to HCA442 where the PPS is tagged by the CTRI in cfc-hca4-saos12. Then the CS4000 is taken back to the CCR where the PPS is again tagged by the CTRI in cfc-ccr-ctpps. The accuracy of the measurement is given by the stability of the CS4000 and the stability of the SPS timing. As the insertion delay between a rising edge detected on the CTRI External Start and its time-stamp is dependent on the CTRI firmware, the calibrations have been estimated for the CTRI firmwares Apr/2008 and Dec/2010.

4 CTRIs under calibration

The PolarRx reference CTRI is located in the CCR, front-end cfc-ccr-ctpps, module 1, SN , CTRI ID NOID, EDA-00530-V2.
The Kicker-pulse and waveform acquisition CTRI is located in the HCA442, front-end cfc-hca4-saos12, module 1, SN, CTRI ID 0x990000001DEFF222, EDA-00530-V3.

5 CTRIs skews

5.1 CTRI skew between firmware Apr/2008 and Dec/2010 External Start Time-tags on Counter 3

The insertion delay between the Apr/2008 and Dec/2010 for the CTRI in HCA442 is estimated by inserting an stable pulse on the External Start and changing the reference CTRI firmware. By using a different CTRP as a source we obtain:

VHDL Apr/2008

```
Mod[1] Int[0x008 3] Time[1303220273:Tue-19/Apr/2011 15:37:53.4730000594] Cntr3 Hptdc: 0x482C9098
Mod[1] Int[0x008 3] Time[1303220273:Tue-19/Apr/2011 15:37:53.4830000594] Cntr3 Hptdc: 0x49B33098
Mod[1] Int[0x008 3] Time[1303220273:Tue-19/Apr/2011 15:37:53.4930000594] Cntr3 Hptdc: 0x4B39D098
...
```

VHDL Dec/2010

```
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:28:34.5730000648] Hptdc: 0x576ED0A6
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:28:34.5830000648] Hptdc: 0x58F570A6
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:28:34.5930000648] Hptdc: 0x5A7C10A6
...
```

We deduce that the Apr/2008 firmware External Start time-tags on counter 3 are delayed by $5.4ns$ respect to the Dec/2010 firmware.

$$\delta^{VHDL2008-VHDL2010}_{ExtStartC3-ExtStartC3} = -5.4ns \pm 0.8ns \tag{5}$$

5.2 CTRI skew between External Start Time-tags on Counter 1 and External Clock Time-tags on Counter 2 VHDL 2008

Some delay calibrations have been made respect to the CCR CTRI External Start and the HCA442 CTRI External Start, while the actual time transfer between both CTRIs is made between the CCR CTRI External Clock and the HCA442 CTRI External Start. This skew has been calculated by connecting both inputs to the same output of a second CTRI with two 0.5ns parallel cables.

```
[1]Ptm:10001[Ctm:320(24:0a:ffff)][Chn:1 Str:Ext1 Mde:Mult Clk:1KHz 0#0 BusOut]
----------
[2]Ptm:10002[Ctm:320(24:0a:ffff)][Chn:2 Str:Self Mde:Mult Clk:Ext1 1#39 BusOut]

Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.1700000484] Hptdc: 0x19F0A07C
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.2700000750] Queued: 1 Hptdc: 0x2932E0C0
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.2700000734] Hptdc: 0x2932E0BC
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.3700000688] Queued: 1 Hptdc: 0x387520B0
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.3700000664] Hptdc: 0x387520AA
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Wed-20/Apr/2011 13:26:09.4700000539] Queued: 1 Hptdc: 0x47B7608A
....
```

$$\delta^{VHDL2008}_{ExtStartC1-ExtClkC2} = -1.6ns \pm 0.1ns \tag{6}$$

5.3 CTRI skew between External Start Time-tags on Counter 1 and External Start Time-tags on Counter 3 VHDL 2010

```
Mod[1] Int[0x002 1] Time[1303291677:Wed-20/Apr/2011 11:27:57.3560165789] Cntr1 Queued: 1 Hptdc: 0x3652E5CA
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Wed-20/Apr/2011 11:27:57.3560165844] Hptdc: 0x3652E5D8
Mod[1] Int[0x002 1] Time[1303291677:Wed-20/Apr/2011 11:27:57.4060092125] Cntr1 Queued: 1 Hptdc: 0x3DF3BC20
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Wed-20/Apr/2011 11:27:57.4060092180] Hptdc: 0x3DF3BC2E
Mod[1] Int[0x002 1] Time[1303291683:Wed-20/Apr/2011 11:28:03.3560309250] Cntr1 Queued: 1 Hptdc: 0x36537540
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Wed-20/Apr/2011 11:28:03.3560309305] Hptdc: 0x3653754E
Mod[1] Int[0x002 1] Time[1303291683:Wed-20/Apr/2011 11:28:03.4060004969] Cntr1 Queued: 1 Hptdc: 0x3DF364F8
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Wed-20/Apr/2011 11:28:03.4060005023] Hptdc: 0x3DF36506
```

$$\delta^{VHDL2010}_{ExtStartC1-ExtStartC3} = -5.7ns \pm 0.1ns \tag{7}$$

5.4 CTRI skew between External Start Time-tags on Counter 1 and External Start Time-tags on Counter 3 VHDL 2008

```
Mod[1] Int[0x008 3] Time[1303307753:Wed-20/Apr/2011 15:55:53.8248294539] Cntr3 Hptdc: 0x7DDBE68A
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0013] Time[Wed-20/Apr/2011 15:55:54.8248294547] Queued: 1 Hptdc: 0x7DDBE68C
Mod[1] Int[0x008 3] Time[1303307754:Wed-20/Apr/2011 15:55:54.8248294547] Cntr3 Hptdc: 0x7DDBE68C
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0013] Time[Wed-20/Apr/2011 15:55:55.8248294531] Queued: 1 Hptdc: 0x7DDBE688
Mod[1] Int[0x008 3] Time[1303307755:Wed-20/Apr/2011 15:55:55.8248294523] Cntr3 Hptdc: 0x7DDBE686
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0013] Time[Wed-20/Apr/2011 15:55:56.8248294547] Queued: 1 Hptdc: 0x7DDBE68C
Mod[1] Int[0x008 3] Time[1303307756:Wed-20/Apr/2011 15:55:56.8248294547] Cntr3 Hptdc: 0x7DDBE68C
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0013] Time[Wed-20/Apr/2011 15:55:57.8248294547] Queued: 1 Hptdc: 0x7DDBE68C
...
```

$$\delta^{VHDL2008}_{ExtStartC1-ExtStartC3} = 0.3ns \pm 0.1ns \tag{8}$$

6 27th January 2010

The 27th January 2010 the CS4000 was taken from the CCR to HCA442.The reference CCR CTRI was installed in abpc11665 but the cabling has been preserved when moved to cfc-ccr-ctpps later that year.

At the CCR the CS4000 PPS was connected to the reference CTRI ExtStart:

```
Mod[1] Int[0x002 1] Time[1264582244:Wed-27/Jan/2010 09:50:44.8248192484] Cntr1 Hptdc: 0x7DDB807C
Mod[1] Int[0x002 1] Time[1264582245:Wed-27/Jan/2010 09:50:45.8248192500] Cntr1 Hptdc: 0x7DDB8080
Mod[1] Int[0x002 1] Time[1264582246:Wed-27/Jan/2010 09:50:46.8248192469] Cntr1 Hptdc: 0x7DDB8078
Mod[1] Int[0x002 1] Time[1264582247:Wed-27/Jan/2010 09:50:47.8248192492] Cntr1 Hptdc: 0x7DDB807E
Mod[1] Int[0x002 1] Time[1264582248:Wed-27/Jan/2010 09:50:48.8248192492] Cntr1 Hptdc: 0x7DDB807E
....
```

At HCA442 the PPS was connected to ExtStart

```
Mod[1] Int[0x002 1] Time[1264591595:Wed-27/Jan/2010 12:26:35.8248091617] Cntr1 Hptdc: 0x7DDB1B9E
Mod[1] Int[0x002 1] Time[1264591596:Wed-27/Jan/2010 12:26:36.8248091617] Cntr1 Hptdc: 0x7DDB1B9E
Mod[1] Int[0x002 1] Time[1264591597:Wed-27/Jan/2010 12:26:37.8248091617] Cntr1 Hptdc: 0x7DDB1B9E
Mod[1] Int[0x002 1] Time[1264591598:Wed-27/Jan/2010 12:26:38.8248091617] Cntr1 Hptdc: 0x7DDB1B9E
Mod[1] Int[0x002 1] Time[1264591599:Wed-27/Jan/2010 12:26:39.8248091617] Cntr1 Hptdc: 0x7DDB1B9E
...
```

Back in the CCR we obtain again:

```
Mod[1] Int[0x002 1] Time[1264592632:Wed-27/Jan/2010 12:43:52.8248192445] Cntr1 Hptdc: 0x7DDB8072
Mod[1] Int[0x002 1] Time[1264592633:Wed-27/Jan/2010 12:43:53.8248192461] Cntr1 Hptdc: 0x7DDB8076
Mod[1] Int[0x002 1] Time[1264592634:Wed-27/Jan/2010 12:43:54.8248192445] Cntr1 Hptdc: 0x7DDB8072
Mod[1] Int[0x002 1] Time[1264592635:Wed-27/Jan/2010 12:43:55.8248192461] Cntr1 Hptdc: 0x7DDB8076
...
```

Figure 3 shows the relative position of the time tags. The time-stamps in the CCR CTRI present an intentional ditter of $\pm 2ns$ that helps to filter out the $800ps$ quantification noise. The time delay between the reference CTRI ExtStart in HCA442 and the reference CTRI ExtStart in the CCR has been estimated in:

$$\delta(Jan2010)^{VHDL2008-2008}_{CCRC1-HCA442C1} = 10085.6ns \pm 2ns \tag{9}$$

This result has to be corrected to include the facts that the kicker pulse is tag-ed on counter 3 instead of counter 1 and that the PolarRX PPS is tagged on the ExtClock counter 2, and not with counter 1.

$$\delta(Jan2010)^{VHDL2008-2008}_{CCRC2-HCA442C3} = \delta(Jan2010)^{VHDL2008-2008}_{CCRC1-HCA442C1} - \delta^{VHDL2008}_{ExtStartC1-ExtClkC2} + .. \\ \delta^{VHDL2008}_{ExtStartC1-ExtStartC3} \tag{10}$$

$$\delta(Jan2010)^{VHDL2008-2008}_{CCRC2-HCA442C3} = 10085.6ns - 1.6ns + 0.3ns = 10084.3ns \pm 2ns \tag{11}$$

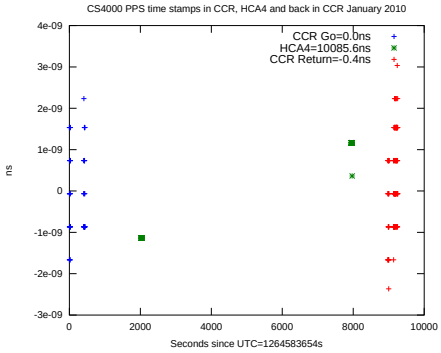

Figure 3: Go and return time-stamps on abpc11665 differ only by 2ns.

7 12th April 2011

The 12th April 2011 the CS4000 was taken from the CCR to HCA442. The reference CTRI in cfc-ccr-ctpps had a firmware version of Apr/2008. The one in cfc-hca4-saos12 had a version from Dec/2010. This has to be taken into account as during the 2010 run, the CTRI in cfc-hca4-saos12 had the Apr/2008 firmware.

The CS4000 PPS was connected to the Ext Clk input of the reference CTRI. The time-stamps obtained from the CTRI were:

```
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0005] Time[Tue-12/Apr/2011 10:18:27.9570770156] Hptdc: 0x9209D228
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0005] Time[Tue-12/Apr/2011 10:18:28.9570770156] Hptdc: 0x9209D228
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0005] Time[Tue-12/Apr/2011 10:18:29.9570770164] Hptdc: 0x9209D22A
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-12/Apr/2011 10:18:30.9570770156] Hptdc: 0x9209D228
.....
```

The CS4000 was taken to HCA4 where we obtain:

```
Mod[1] Int[0x008 3] Time[1302597619:Tue-12/Apr/2011 10:40:19.9570669344] Cntr3 Hptdc: 0x92096D58
Mod[1] Int[0x008 3] Time[1302597620:Tue-12/Apr/2011 10:40:20.9570669344] Cntr3 Hptdc: 0x92096D58
Mod[1] Int[0x008 3] Time[1302597621:Tue-12/Apr/2011 10:40:21.9570669344] Cntr3 Hptdc: 0x92096D58
Mod[1] Int[0x008 3] Time[1302597622:Tue-12/Apr/2011 10:40:22.9570669344] Cntr3 Hptdc: 0x92096D58
....
```

Back at the CCR we obtained:

```
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-12/Apr/2011 10:56:47.9570770164] Hptdc: 0x9209D22A
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-12/Apr/2011 10:56:48.9570770164] Hptdc: 0x9209D22A
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0005] Time[Tue-12/Apr/2011 10:56:49.9570770164] Hptdc: 0x9209D22A
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0005] Time[Tue-12/Apr/2011 10:56:50.9570770180] Hptdc: 0x9209D22E
....
```

The calibration result is:

$$\delta(12Apr2011)^{VHDL2008-2010}_{CCR-HCA442} = 10081ns \pm 2ns \tag{12}$$

Which is valid for the 2011 run.

If the measurement is transferred to the 2008 CTRI firmware, we get:

$$\delta(12Apr2011)^{VHDL2008-2008}_{CCR-HCA442} = \delta(12Apr2011)^{VHDL2008-2010}_{CCRC2-HCA442C3} - \delta^{VHDL2008-VHDL2010}_{ExtStartC3-ExtStartC3} \tag{13}$$

If the measurement is transfered to the

$$\delta(12Apr2011)^{VHDL2008-2008}_{CCR-HCA442} = 10081ns + 5.4ns = 10086.4 \pm 2ns \tag{14}$$

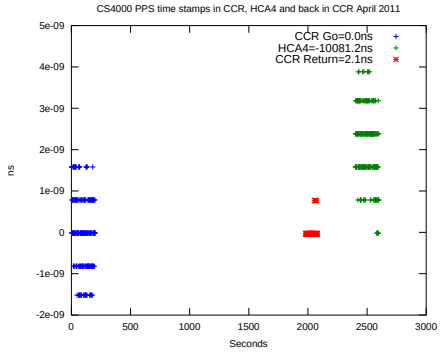

Figure 4: Go and return time-stamps on cfc-ccr-ctpps differ by 2ns.

Which is coherent with the measurements of 2010.

8 19th April 2011

A second CTRI was connected to the SPS timing in cfc-ccr-ctpps. This conexion representes an increment of the cable capcitance, which induces an increase in the transmision delay to cfc-ccr-ctpps. This in turn represents a decrease in the measured delay between the CCR and HCA442 of 4.2ns.

The calibration was repeated, this time changing the firmware from 2010 to 2008 in HCA442. The traveling CS4000 is connected to External Clock (PPSSEP-CTPPS), Counter 2, whereas a fixed CS4000 is connected to External Start (PPSXLI), Counter 1. The time tags in the CCR are:

```
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:47.9570770938] Hptdc: 0x9209D2F0
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:48.8248294328] Hptdc: 0x7DDBE654
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:48.9570770945] Hptdc: 0x9209D2F2
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:49.8248294336] Hptdc: 0x7DDBE656
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:49.9570770930] Hptdc: 0x9209D2EE
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:50.8248294320] Hptdc: 0x7DDBE652
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 15:05:50.9570770945] Hptdc: 0x9209D2F2
....
```

The CS4000 is taken to the HCA442 where it is connected to the External Start Counter 3. The obtained time-tags are:

VHDL Dec/2010

```
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:26:32.9570670188] Hptdc: 0x92096E30
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:26:33.9570670188] Hptdc: 0x92096E30
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:26:34.9570670195] Hptdc: 0x92096E32
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:26:35.9570670188] Hptdc: 0x92096E30
Mod[1] PTIM[10001:RtAqn:SEX.CNGS-SAOS08] Cntr[3] Frme[0x24070012] Time[Tue-19/Apr/2011 15:26:36.9570670188] Hptdc: 0x92096E30
...
```

VHDL Apr/2008

```
Mod[1] Int[0x008 3] Time[1303220178:Tue-19/Apr/2011 15:36:18.9570670125] Cntr3 Hptdc: 0x92096E20
Mod[1] Int[0x008 3] Time[1303220179:Tue-19/Apr/2011 15:36:19.9570670125] Cntr3 Hptdc: 0x92096E20
Mod[1] Int[0x008 3] Time[1303220180:Tue-19/Apr/2011 15:36:20.9570670125] Cntr3 Hptdc: 0x92096E20
Mod[1] Int[0x008 3] Time[1303220181:Tue-19/Apr/2011 15:36:21.9570670125] Cntr3 Hptdc: 0x92096E20
Mod[1] Int[0x008 3] Time[1303220182:Tue-19/Apr/2011 15:36:22.9570670125] Cntr3 Hptdc: 0x92096E20
...
```

Back at the CCR we obtain.

```
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:11.8248294320] Hptdc: 0x7DDBE652
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:11.9570770938] Hptdc: 0x9209D2F0
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:12.8248294320] Hptdc: 0x7DDBE652
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:12.9570770961] Hptdc: 0x9209D2F6
Mod[1] PTIM[10001:RtAqn:SX.PPSXLI-CTPPS] Cntr[1] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:13.8248294336] Hptdc: 0x7DDBE656
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0012] Time[Tue-19/Apr/2011 16:02:13.9570770938] Hptdc: 0x9209D2F0
...
```

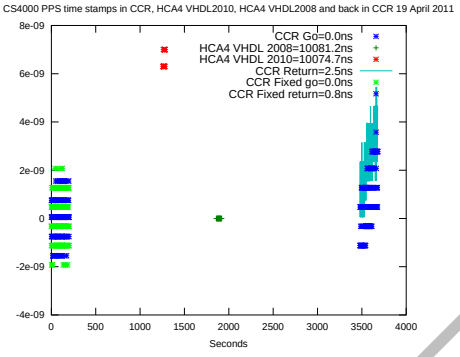

Figure 5: Calibration after connecting second CTRI to the SPS timing in ctf-ccr-ctpps.

$$\delta(19Apr2011)^{VHDL2008-2010}_{CCR-HCA442} = 10075ns \pm 2ns \quad (15)$$

$$\delta(19Apr2011)^{VHDL2008-2008}_{CCR-HCA442} = 10081ns \pm 2ns \quad (16)$$

9 4ns step induced by the connexion of a second CTRI

The 19th of April the second CTRI that was in cfc-ccr-ctpps was desconected from the LHC timing and connected to the SPS timing to monitor a PPS sent from HCA442. Figures 6 and 7 show the moment of the conexion. The phase measurement has been repeated with the fiber calibration being logged in CFC-CCR-CTPPS.XLI since 2011-07-28 15:19:19. We can see that when the SPS timing is disconected from the second CTRI, the timing in the CTRI logging the septentrio PPS is advanced by 4.1ns.

10 Fiber Calibration

An additional fiber link has been added in parallel to the GMT link between cfc-ccr-ctpps and cfc-hca4-saos12. First a pulse is sent from the CCR to HCA442 and tagged simultaneously in both places. Then the optical receiver and transmitters are exchanged and the operation is repeated in a reversed path. The calibration path delay should be the same in both directions as the receiver and transmitter are identical in both cases. There is still an incertitude of +/-800ps in this method due to the fact that it is the CTRI itself that is generating and tagging the pulse using the same clock. Figures 9 and 10 describe the measurement setup. The calibration path has been left permanently configured as in 10. The time-tags in cfc-ccr-ctpps are stored in the permanent database to observe any possible drift in the transmission delays.

From Figures 9 and 10 we can write

CCR to HCA442:

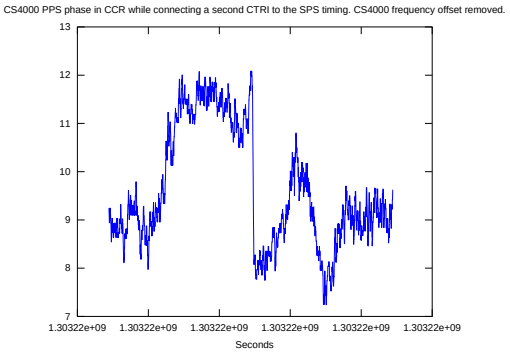

Figure 6: Phase jump at the conexion of an spare CTRI the 19th April 2011.

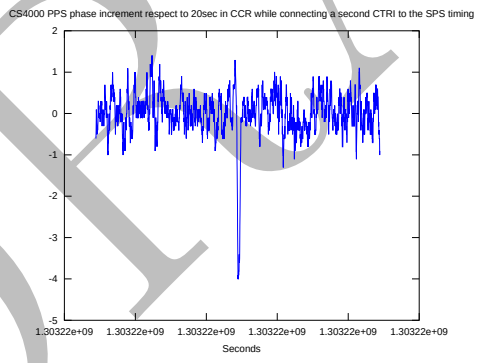

Figure 7: Phase jump increment at the conexion of an spare CTRI the 19th April 2011.

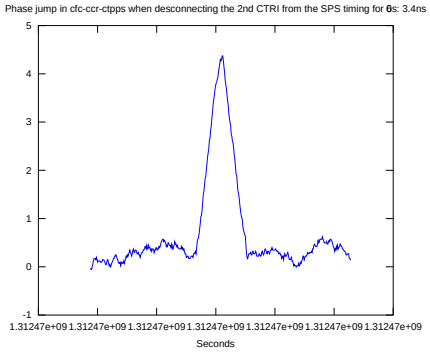

Figure 8: 4ns phase jump during the unconnexion of an spare CTRI.

$$t_{c1} = t_1 + A \tag{17}$$

$$t_{h1} = (t_1 + \beta) + B \tag{18}$$

HCA442 to CCR:

$$t_{c2} = (t_2 + \beta) + A \tag{19}$$

$$t_{h2} = t_2 + B \tag{20}$$

Where t_{c1} and t_{h1} are the time-tags for a pulse generated at the CCR and received at HCA442 respectively. t_{c2} and t_{h2} are the time-tags for a pulse traveling from HCA442 to the CCR. t_1, and t_2 are the generation pulse time-stamps respect to an ideal time base. β is the calibration path transmission delay, A and B are the offsets of the timing receivers respect to this ideal time base. We are interested in finding the time offset between the timing receiver in the CCR and HCA442, δ_3:

$$\delta_3 = A - B \tag{21}$$

$$t_{h1} - t_{c1} = \beta - \delta_3 \tag{22}$$

$$t_{c2} - t_{h2} = \beta + \delta_3 \tag{23}$$

$$\delta_3 = ((t_{c2} - t_{h2}) - (t_{h1} - t_{c1}))/2 \tag{24}$$

$$\beta = ((t_{c2} - t_{h2}) + (t_{h1} - t_{c1}))/2 \tag{25}$$

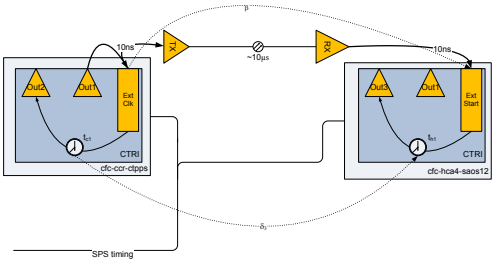

Figure 9: Fiber calibration path from CCR to HCA442.

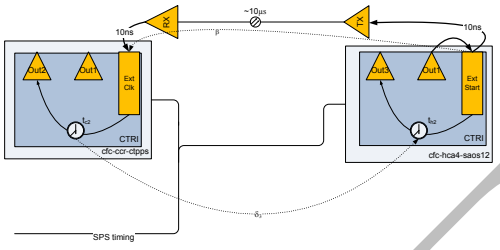

Figure 10: Fiber calibration path from HCA442 to CCR.

11 Fiber Calibration July 2011

For the CCR to HCA442 transmission path we obtain at the CCR (t_{c1}):

```
.........
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0010] Time[Thu-28/Jul/2011 16:35:21.9999109992] Hptdc: 0x989305FE
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0010] Time[Thu-28/Jul/2011 16:35:22.9999109977] Hptdc: 0x989305FA
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0010] Time[Thu-28/Jul/2011 16:35:23.9999109992] Hptdc: 0x989305FE
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0010] Time[Thu-28/Jul/2011 16:35:24.9999109984] Hptdc: 0x989305FC
.........
```

And at HCA442 (t_{h1}):

```
....
Mod[1] Int[0x008 3] Time[1311863719:Thu-28/Jul/2011 16:35:19.9999109984] Cntr3 Hptdc: 0x989305FC
Mod[1] Int[0x008 3] Time[1311863720:Thu-28/Jul/2011 16:35:20.9999109977] Cntr3 Hptdc: 0x989305FA
Mod[1] Int[0x008 3] Time[1311863721:Thu-28/Jul/2011 16:35:21.9999109984] Cntr3 Hptdc: 0x989305FC
Mod[1] Int[0x008 3] Time[1311863722:Thu-28/Jul/2011 16:35:22.9999109977] Cntr3 Hptdc: 0x989305FA
Mod[1] Int[0x008 3] Time[1311863723:Thu-28/Jul/2011 16:35:23.9999109984] Cntr3 Hptdc: 0x989305FC
Mod[1] Int[0x008 3] Time[1311863724:Thu-28/Jul/2011 16:35:24.9999109977] Cntr3 Hptdc: 0x989305FA
Mod[1] Int[0x008 3] Time[1311863725:Thu-28/Jul/2011 16:35:25.9999109977] Cntr3 Hptdc: 0x989305FA
.......
```

For the HCA442 to CCR transmission path we obtain at HCA442 (t_{h2}):

```
...
Mod[1] Int[0x008 3] Time[1311865676:Thu-28/Jul/2011 17:07:56.0000000367] Cntr3 Hptdc: 0x0000005E
Mod[1] Int[0x008 3] Time[1311865677:Thu-28/Jul/2011 17:07:57.0000000367] Cntr3 Hptdc: 0x0000005E
Mod[1] Int[0x008 3] Time[1311865678:Thu-28/Jul/2011 17:07:58.0000000367] Cntr3 Hptdc: 0x0000005E
Mod[1] Int[0x008 3] Time[1311865679:Thu-28/Jul/2011 17:07:59.0000000367] Cntr3 Hptdc: 0x0000005E
Mod[1] Int[0x008 3] Time[1311865680:Thu-28/Jul/2011 17:08:00.0000000367] Cntr3 Hptdc: 0x0000005E
Mod[1] Int[0x008 3] Time[1311865681:Thu-28/Jul/2011 17:08:01.0000000367] Cntr3 Hptdc: 0x0000005E
...
```

At the CCR we obtain (t_{c2}):

```
...
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:53.0000201930] Hptdc: 0x0000C9EE
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:54.0000201930] Hptdc: 0x0000C9EE
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:55.0000201922] Hptdc: 0x0000C9EC
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:56.0000201914] Hptdc: 0x0000C9EA
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:57.0000201906] Hptdc: 0x0000C9E8
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:58.0000201922] Hptdc: 0x0000C9EC
```

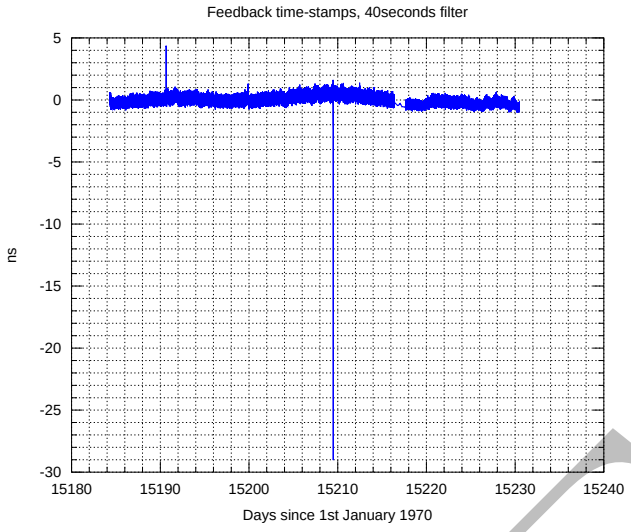

Figure 11: Feedback timestamp with a running window filter of 40seconds. Phase jump around day 15190 was due to the deconexion of the auxiliar CTRI for a test. The phase jump around day 15210 was due to an intervention. There were no CNGS extractions during that time. The gap around day 15217 was due to a technical stop in the CERN complex.

```
Mod[1] PTIM[10002:RtAqn:SX.PPSSEP-CTPPS] Cntr[2] Frme[0x240A0008] Time[Thu-28/Jul/2011 17:07:59.0000201914] Hptdc: 0x0000C9EA
...
```

By averaging these values we obtain:

$$\delta(28July2011)^{VHDL2008-2010}_{CCRC2-HCA442C3} = 10077.8ns \tag{26}$$

$$\beta(28July2011)^{VHDL2008-2010}_{CCRC2-HCA442C3} = 10077.5ns \tag{27}$$

12 Fiber feedback stability

Figure 11 and 12 show the evolution of the feedback timestamps since 29th July until 13th September 2011. The 4ns peak observed in Figure 11 was produced by the disconexion of the SPS timing in the 2nd CTRI in cfc-ccr-ctpps. Figure 12 represent the same timestamps filtered with a one hour running window filter. Day to day variations due to temperature changes are easyly observed. July ended with temperatures oscillating between 20°C to 13°C, and august ends with temperatures between 20°C-33°C.

13 Acknowledgements

I would like to acknowledge the help of Javier Serrano, Benjamin Ninet, Giulia Brunetti and Dario Autiero in this measurement.

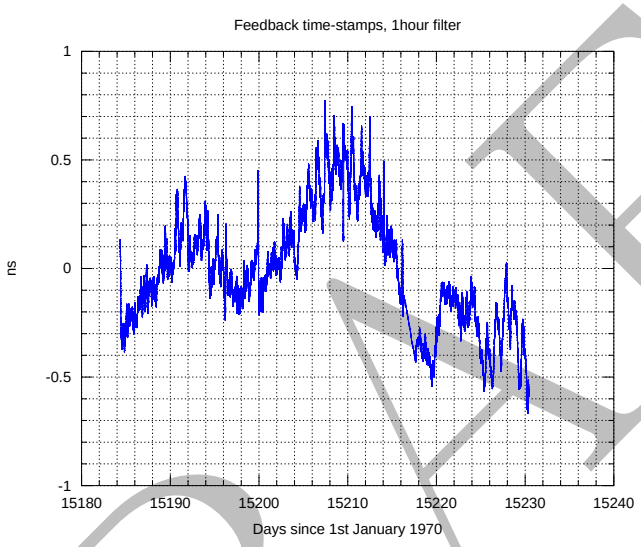

Figure 12: Feedback timestamp with a running window filter of 1hour